

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1        1.    (Currently Amended) A method of exporting from a data  
2 processor emulation information including emulation control  
3 information and emulation data, comprising:  
4        arranging the emulation information into fixed length  
5 information blocks;  
6        outputting a sequence of the information blocks from the data  
7 processor via a plurality of terminals of the data processor; and  
8        said arranging step including providing some of the  
9 information blocks of the sequence with relative proportions of  
10 emulation control information and emulation data that differ from  
11 the relative proportions of emulation control information and  
12 emulation data in other blocks of the sequence.

2 and 3.    (Canceled)

1        4.    (Currently Amended) The method of Claim 3, further  
2 comprising:  
3        storing comparison data;  
4        comparing respective sections of emulation data with the  
5 stored comparison data; and  
6        wherein the emulation control information in one of the  
7 information blocks includes a compression map indicative of whether  
8 the sections of the emulation data match the stored comparison  
9 data.

1        5.    (Currently Amended) The method of Claim 1, wherein the  
2 emulation data in one of the information blocks ~~represents~~  
3 ~~operations of a clock used by~~ includes bits indicating whether the

4 data processor ~~for performing~~ performed data processing operations  
5 during a corresponding clock cycle.

6 to 12. (Canceled)

1 13. (Currently Amended) An integrated circuit device,  
2 comprising:  
3 a data processing portion for performing data processing  
4 operations;  
5 an emulation information collector coupled to said data  
6 processing portion for receiving emulation data therefrom, said  
7 collector operable for arranging the emulation data and associated  
8 emulation control information into fixed length information blocks;  
9 a plurality of terminals coupled to said collector for  
10 permitting said collector to communicate with an emulation  
11 controller located externally of said integrated circuit device;  
12 and  
13 said collector operable for providing to said terminals a  
14 sequence of said information blocks to be output to the emulation  
15 controller, said collector further operable for providing some of  
16 the information blocks of the sequence with relative proportions of  
17 emulation control information and emulation data that differ from  
18 the relative proportions of emulation control information and  
19 emulation data in other blocks of the sequence.

14 and 15. (Canceled)

1 16. (Currently Amended) The device of Claim ~~15~~ 13, further  
2 comprising:  
3 a comparison data register storing comparison data;  
4 a comparator connected to said comparison data register and  
5 receiving emulation data generating an indication of a match

6 between corresponding sections of said comparison data and said  
7 emulation data; and  
8 wherein the emulation control information in one of the  
9 information blocks includes a compression map indicative of whether  
10 the sections of the emulation data match the stored comparison  
11 data.

1 17. (Currently Amended) The device of Claim 13, wherein the  
2 emulation data in one of the information blocks ~~represents~~  
3 ~~operations of a clock used by~~ includes bits indicating whether the  
4 data processor ~~for performing~~ performed data processing operations  
5 during a corresponding clock cycle.

18 to 24. (Canceled)

1 25. (Currently Amended) A data processing system, comprising:  
2 an integrated circuit, including a data processing portion for  
3 performing data processing operations;  
4 an emulation controller located externally of said integrated  
5 circuit and coupled to said integrated circuit for controlling  
6 emulation operations of said integrated circuit;  
7 said integrated circuit including an emulation information  
8 collector coupled to said data processing portion for receiving  
9 emulation data therefrom, said collector operable for arranging the  
10 emulation data and associated emulation control information into  
11 fixed length information blocks; and  
12 said collector coupled to said emulation controller for  
13 permitting said collector to communicate with said emulation  
14 controller, said collector operable for outputting to said  
15 emulation controller a sequence of said information blocks, said  
16 collector further operable for providing some of the information  
17 blocks with relative proportions of emulation control information

18 and emulation data that differ from the relative proportions of  
19 emulation control information and emulation data in other blocks of  
20 the sequence.

26 and 27. (Canceled)